IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Attorney Docket Number 15483US02

In re Application of:	)	
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Ramadas Lakshmikanth Pai	)	**ELECTRONICALLY FILED**
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Serial No.: 10/816,118	)	
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Filing Date: 4/1/2004	)	
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Examiner: Anner N. Holder	)	
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Confirmation No.: 8484	)	
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Art Unit No. 2621	)	
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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Sir:

This is an appeal from the Office Action made Final mailed October 23, 2009. A Notice of Appeal and Pre-Appeal Brief were filed with the United States Patent and Trademark Office on March 23, 2010. On May 24, 2010, Examiner advised Appellant to proceed to Appeal.

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I. REAL PARTY IN INTEREST

Broadcom Corporation, a corporation having a place of business at 5300 California Drive, Irvine California 92617, has acquired the entire right, title, and interest in and to the invention, the application, and any and all patents to be obtained therefrom.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-3, 5, 7-9 and 15 are rejected under 35 U.S.C. 103(a) as anticipated by U.S. Patent 6,310,921 to Yoshioka ("Yoshioka") in view of U.S. Patent 5,706,059 ("Ran").

Claims 4, 6, and 10-14 are cancelled without prejudice.

Claims 1-3, 5, 7-9, and 15 are appealed.

IV. STATUS OF AMENDMENTS

There are no amendments pending in the present application.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to a video request manager comprising:

a first state machine (Specification at 14, Lines 14-15, Figure 4, 405R) for commanding a memory controller

(Figure 4, 309) to fetch reference pixels for a first portion of a picture; and

a second state machine (Specification at 14, Lines 14-15, Figure 4, 405W) for commanding a memory controller (Figure 4, 309) to write a second portion of the picture, wherein the second state machine loads the memory controller with the second portion while the memory controller fetches the reference pixels (Specification at 14, line 31 – p. 15, line 3).

Claim 5 is directed to a circuit for decoding video data, said circuit comprising:

a motion vector address computer (Specification at 13, lines 23-28, Figure 3, 308) for calculating at least one address for reference pixels for a first portion of a picture;

a motion compensator (Specification at 14, lines 23-27, Figure 4, motion compensator 312)for decoding another portion of the picture;

a video request manager (Specification at 14, lines 10-11, Figure 4, 310) comprising:

a first state machine (Specification at 14, lines 14-15, Figure 4, 405R) for issuing a command to fetch reference pixels for a first portion of a picture (Specification at 14, lines 28-30); and

a second state machine (Specification at 14, lines 14-15, Figure 4, 405W) for issuing a command to write a second portion of the picture (Specification at 14, lines 28-30);

a memory controller (Figure 4, memory controller 309) for fetching the reference pixels after the first state machine issues the command, and writing the second portion of the picture after the second state machine issues the command, and wherein the memory controller loads the second portion of the picture while fetching the reference pixels.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3, 5, 7-9, and 15 as obvious from Yoshioka in view of Ran.

VII. ARGUMENT: CLAIMS 1

Claim 1 is recited below:

> A video request manager comprising:
>
> a first state machine for commanding a memory controller to fetch reference pixels for a first portion of a picture; and
>
> a second state machine for commanding a memory controller to write a second portion of the picture, wherein the second state machine loads the memory controller with the second portion while the memory controller fetches the reference pixels.

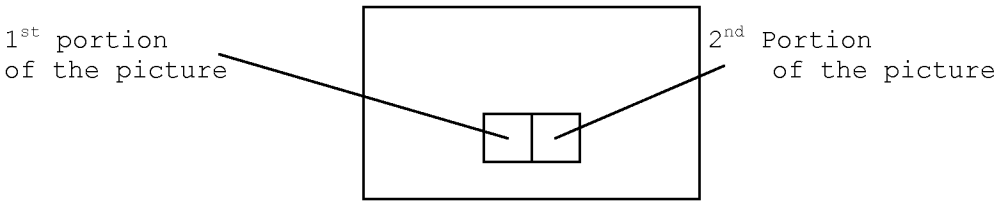
Claim 1 was rejected under 35 U.S.C. 103(a) as being obvious from the combination of Yoshioka and Ran. Appellant respectfully submits that the rejection to claim 1 should be reversed because the combination of Yoshioka and Ran does not teach "fetching reference pixels for a first portion of a picture" and "load the memory controller of a picture while the memory controller fetches the reference pixels" and because Yoshioka and Ran cannot be combined in the manner suggested in the Office Action.

A. THE REJECTION TO CLAIM 1 SHOULD BE REVERSED BECAUSE THE COMBINATION OF YOSHIOKA AND RAN DOES NOT TEACH "FETCHING REFERENCE PIXELS FOR A FIRST PORTION OF A PICTURE" AND "LOADS THE MEMORY CONTROLLER WITH THE SECOND PORTION WHILE THE MEMORY CONTROLLER FETCHES THE REFERENCE PIXELS".

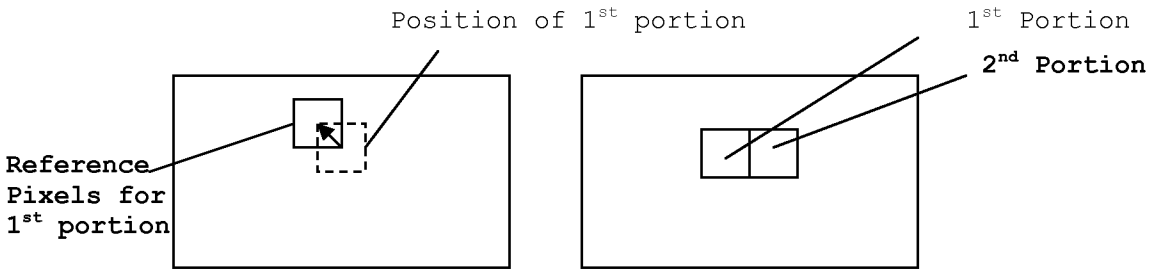
Notably, claim 1 recites among other limitations, "fetch reference pixels for a first portion of a picture" and "loads the memory controller with the second portion while the memory controller fetches the reference pixels".

From the claim language, the "first portion" and the "second portion" are from the same picture. In certain video compression standards such as MPEG-2, frames are divided into portions, known as blocks. Specification 0020.

The following description is provided for illustrative purposes:



However, what is fetched is "*reference pixels* for a first portion of a picture". MPEG-2 also uses motion compensation/estimation. In motion compensation/estimation the blocks are compared to pixels of *other* frames (reference frames). When an appropriate (most similar, i.e. containing the same object(s)) portion of a reference frame is found, the differences between the portion of the reference frame (reference pixels) and the block are encoded. **The difference between the reference pixels and the block, the prediction error,** is encoded using the discrete cosine transformation, thereby resulting in frequency coefficients. The frequency coefficients are then quantized and Huffman coded. **The location of the reference pixels in the reference frame is recorded as a motion vector.** 0022-0023.



Reference Frame

In Assignee's claimed invention, the "second state machine loads the memory controller with the **second portion** while the memory controller fetches the **reference pixels**". "[T]he reference pixels" claims antecedent basis to the **first portion** of the picture, not the second portion. The claimed reference pixels for the first portion of the picture and the second portion of the picture in exemplary case described above are bolded. The first portion would be coded as the difference between the reference pixels for the first portion and the first portion. The first portion is decoded by adding the difference to the reference pixels.

The Office Action indicates that:

> Yoshioka teaches a video request manager [Fig. 3; Fig. 4; Fig. 16] comprising: a first state machine for commanding a memory controller to fetch reference pixels for a first portion of a picture; [Fig. 4; Fig. 16; Col. 11 Line 64 – Col. 12 Line 7; Col. 13 Line 56 – Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14] and a second state machine for commanding a memory controller to write a second portion of the picture [fig. 4; Col. 13 Line 56 – Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14, 20-27] memory controller fetches the reference pixels [Col. 14 Lines 38-45]
>
> Yoshioka teaches pipeline processing in decoding including read/write function that is divided into two sections [see fig. 15 A&B] allowing them to operate in tandem.

Office Action at 3-4.

Although the Office Action indicates that "Yoshioka teaches pipeline processing in decoding including read/write function that is divided into two sections [see fig. 15 A&B] allowing them to operate in tandem", Assignee respectfully submits that the foregoing does not teach

"fetch **reference pixels for a first portion** of a picture" and "loads the memory controller with the **second portion** while the memory controller fetches the reference pixels".

Assignee calls Examiner's attention to Yoshioka, Figure 4, and Col. 14, Lines 38-45, which was cited by Examiner as teaching "memory controller fetches the reference pixels".

> More specifically, for P-pictures or B-Pictures the pixel read/write unit 11 extracts **a rectangle area indicated by the motion vector** from the decoded reference frame in the external memory 3 via the memory controller 6 and **blends the rectangle area with the block** processed by the pixel calculation unit 10 **to obtain an original block image.** The decode result given by the pixel read/write unit 11 here is stored in the external memory 3 via the memory controller 6.

From the foregoing, note that the "rectangle area indicated by the motion vectors from the decoded reference frame in the external memory" and "the block" are blended together to obtain the original block image. In other words, the rectangular block are the reference pixels for the block processed by the pixel calculation unit 10.

However, what is claimed is "fetch **reference pixels for a first portion** of a picture" and "loads the memory controller with the ***second*** **portion**" in contrast with fetching **reference pixels for a first portion** and loading the **first portion.**

> In Figure 10, Col. 18, Lines 6-27 (Emphasis Added)
>
> The read/write control unit 79 performs the MC on the block data inputted via the buffer 201 using the buffers A to D, and transfers the decoded images to the external memory 3 in units of two blocks. More specifically, the read/write control unit 79 controls the memory controller 6 to read out rectangle areas corresponding to the present two blocks from the reference frame stored in the

> external memory 3 in accordance with the motion vectors set during the header analysis by the processor 7. As a result, the data of the rectangle areas corresponding to the two blocks indicated by the motion vectors are stored in the buffer A or the buffer B. Following this, the blending unit 76 performs the halfpel interpolation on the rectangle areas of the two blocks, depending on the picture type (whether the I-pictures, the P-pictures, or the B-pictures). The read/write control unit 79 calculates pixel values of the present two blocks by blending the block data inputted via buffer 201 with the halfpel interpolated rectangle areas (by adding the block data to the rectangle area), and then stores the calculated pixel values in the buffer B. These decoded blocks stored in the buffer B are transferred to the external memory 3 via the memory controller 6.

Similarly, contrast reference pixels for a block and the block, with reference pixels for a first block and a second block.

Accordingly, for at least the foregoing reasons, Appellant respectfully requests that the rejection to claim 1 and its dependent claims be REVERSED.

B. THE REJECTION OF CLAIM 1 SHOULD BE REVERSED BECAUSE IT WOULD NOT BE OBVIOUS TO MODIFY YOSHIOKA WITH THE TEACHINGS OF RAN

Finally, even Yoshioka was deemed to teach "fetch reference pixels for a first portion of a picture" and "write a second portion of the picture", Assignee still maintains traverse. Although the Office Action indicates that "It is well known in the art that memory is capable of performing simultaneous read/write operations…" Office Action at 2-3, it would not be possible to apply to

Yoshioka. Note that Yoshioka, "extracts a rectangle area indicated by the motion vector" and that "The decode result given by the pixel read/write unit 11 here is stored in the external memory 3 via the memory controller 6."

However, even in view of the teachings of Ran, Yoshioka could not be modified to perform the foregoing simultaneously, because "the decode result … stored in the external memory 3", only becomes available when "the rectangle area" is blended with the block. Thus, the rectangle area has to be extracted before the decode result can be stored in the external memory 3. Accordingly, Assignee respectfully traverses that it "would have been obvious … to incorporate the simultaneous read/search and write teaching of Ran with the device of Yoshioka".

Accordingly, Appellant respectfully requests that the rejection to claim 1 and its dependents be REVERSED.

VIII. ARGUMENT: CLAIMS 5

Claim 5 is copied below:

> 5. (Currently Amended) A circuit for decoding video data, said circuit comprising:
>
> a motion vector address computer for calculating at least one address for reference pixels for a first portion of a picture;
>
> a motion compensator for decoding another portion of the picture;
>
> a video request manager comprising:
>
> a first state machine for issuing a command to fetch reference pixels for a first portion of a picture; and
>
> a second state machine for issuing a command to write a second portion of the picture;
>
> a memory controller for fetching the reference pixels after the first state machine issues the command, and writing the second portion of the picture after the second state machine issues the command, and wherein the memory controller loads the second portion of the picture while fetching the reference pixels.

Claim 5 was rejected under 35 U.S.C. 103(a) as being obvious from the combination of Yoshioka and Ran. Appellant hereby incorporates Section VII by reference and submits that the rejection to claim 5 and its dependents should be REVERSED for the reasons stated therein.

CONCLUSION

For the foregoing reasons, claims 1-18 are distinguishable over the prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: September 24, 2010

Respectfully submitted,

/Mirut Dalal/

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CLAIMS APPENDIX

1. A video request manager comprising:

a first state machine for commanding a memory controller to fetch reference pixels for a first portion of a picture; and

a second state machine for commanding a memory controller to write a second portion of the picture, wherein the second state machine loads the memory controller with the second portion while the memory controller fetches the reference pixels.

2. The video request manager of claim 1, wherein the second state machine commands the memory controller to write the second portion, such that a resource contention occurs between the command to fetch reference pixels, and the command to write the second portion.

3. The video request manager of claim 2, wherein the second state machine commands the memory controller to write the second portion, such that the command to fetch reference pixels is given priority during the resource contention.

4. (Cancelled).

5. A circuit for decoding video data, said circuit comprising:

a motion vector address computer for calculating at least one address for reference pixels for a first portion of a picture;

a motion compensator for decoding another portion of the picture;

a video request manager comprising:

a first state machine for issuing a command to fetch reference pixels for a first portion of a picture; and

a second state machine for issuing a command to write a second portion of the picture;

a memory controller for fetching the reference pixels after the first state machine issues the command, and writing the second portion of the picture after the second state machine issues the command, and wherein the memory controller loads the second portion of the picture while fetching the reference pixels.

6. (Cancelled).

7. (Previously Presented) The circuit of claim 5, wherein the memory controller further comprises:

an arbiter for causing the memory controller to give priority to the command to fetch the reference pixels.

8. (Previously Presented) The circuit of claim 5, wherein the memory controller further comprises:

a write buffer for storing the second portion of the picture while fetching the reference pixels.

9. (Original) The circuit of claim 8, wherein the memory controller writes the second portion of the picture from the write buffer to a memory system, after fetching the reference pixels.

10-14. (Cancelled).

15. (Previously Presented) The video request manager of claim 1, wherein the second state machine loads the memory controller with the second portion reconstructed from decoding while the memory controller fetches the reference pixels.

EVIDENCE APPENDIX

There are no pages in this appendix

RELATED PROCEEDINGS APPENDIX

There are no pages in this Appendix.